Examiner's Amendment

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no lather than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Robert A. Greenberg (Registration No. 44,133) on 6/17/2008.

3. Amend the following claims:

1. (currently amended) A computer implemented method comprising:

receiving a plurality of descriptors at a controller, wherein the descriptors are received in a first order and wherein each descriptor includes a command and a memory address identifying a memory location external to the descriptor to which a completion status of the command will be written upon completion of the command;

executing the command; and

upon completion of a command included in a respective descriptor, writing a completion status value for the command to the memory address external to the respective descriptor;

wherein at least some of the descriptors comprise commands executed by one of multiple encryption units implementing different respective encryption algorithms;

wherein the multiple encryption units comprise (1) an Advanced Encryption Standard (AES) encryption engine; and (2) a Data Encryption Standard (DES) engine; and

wherein the controller comprises logic to write a second completion status to a memory address external to a second descriptor prior to writing a first completion status to a memory address external to a first descriptor and wherein controller logic to execute a command in the first descriptor is initiated before execution of a command in the second descriptor is initiated.

2. (cancelled)

3. (previously presented) The computer implemented method of claim 1 wherein the memory address included in the descriptor is an absolute address.

4. (previously presented) The computer implemented method of claim 1 wherein the memory address included in the descriptor is an offset from a base memory address.

5. (cancelled).

6. (original) The computer implemented method of claim 1 wherein the commands are grouped into categories, and the completion status of commands in each category are written to different blocks of memory locations.

7. (original) The computer implemented method of claim 6 wherein the commands are grouped into categories depending on their execution times.

8. (original) The computer implemented method of claim 6 wherein the commands are grouped into categories depending on which of a plurality of resources executes them.

9. (original) The computer implemented method of claim 6 wherein each block of memory comprises a plurality of memory locations.

10. (original) The computer implemented method of claim 6 wherein each block of memory comprises a single memory location.

11. (original) The computer implemented method of claim 1 wherein the value to be written indicates the command's original location.

12. (currently amended) An article of manufacture comprising:

a ~~machine-readable~~ storage medium having instructions stored thereon to be executed by a processor to:

receive a plurality of descriptors at a controller, wherein the descriptors are received in a first order and wherein each descriptor includes a command and a memory address identifying a memory location external to the descriptor to which a completion status of the command will be written upon completion of the command;

execute the command; and

upon completion of a command included in a respective descriptor, write a completion status value for the command to the memory address external to the respective descriptor;

wherein at least some of the descriptors comprise commands executed by one of multiple encryption units implementing different respective encryption algorithms;

wherein the multiple encryption units comprise (1) an Advanced Encryption Standard (AES) encryption engine; and (2) a Data Encryption Standard (DES) engine; and

wherein the controller comprises logic to write a second completion status to a memory address external to a second descriptor prior to writing a first completion status to a memory address external to a first descriptor and wherein controller logic to execute a command in the first descriptor is initiated before execution of a command in the second descriptor is initiated.

13. (cancelled)

14. (previously presented) The article of manufacture of claim 12 wherein the memory address included in the descriptor is an absolute address.

15. (previously presented) The article of manufacture of claim 12 wherein the memory address included in the descriptor is an offset from a base memory address.

16. (previously presented) The article of manufacture of claim 12 wherein the value to be written indicates the command's original location.

17. (original) The article of manufacture of claim 12 wherein each command is stored in a first memory location, and the completion status of each command is written to a second memory location different from the first memory location.

18. (original) The article of manufacture of claim 12 wherein the commands are grouped into categories, and the completion status of commands in each category are written to different blocks of memory locations.

19. (original) The article of manufacture of claim 18 wherein the commands are grouped into categories depending on their execution times.

20. (original) The article of manufacture of claim 18 wherein the commands are grouped into categories depending on which of a plurality of resources executes them.

21. (original) The article of manufacture of claim 18 wherein each block of memory comprises a plurality of memory locations.

22. (original) The article of manufacture of claim 12 wherein each block of memory comprises a single memory address.

23. (currently amended) An apparatus comprising:

a controller having a processor to:

accept a plurality of descriptors, wherein the descriptors are received in a first order and wherein each descriptor includes a command and a memory address identifying a memory location external to the descriptor to which a completion status of the command will be written upon completion of the command;

execute ~~executing~~ the command; and

upon completion of a command included in a respective descriptor, ~~writing~~ write a completion status for value the command to the memory address external to the respective descriptor;

wherein at least some of the descriptors comprise commands executed by one of multiple encryption units implementing different respective encryption algorithms;

wherein the controller comprises the multiple encryption units; ~~and~~

wherein the multiple encryption units comprise (1) an Advanced Encryption Standard (AES) encryption engine; and (2) a Data Encryption Standard (DES) engine; and

wherein the controller comprises logic to write a second completion status to a memory address external to a second descriptor prior to writing a first completion status to a memory address external to a first descriptor and wherein controller logic to execute a command in the first descriptor is initiated before execution of a command in the second descriptor is initiated.

24. (cancelled)

25. (previously amended) The apparatus of claim 23 wherein the commands are grouped into categories, and wherein the completion status of commands in each category are written to different blocks of memory locations.

26. (previously amended) The apparatus of claim 25 wherein each block of memory locations comprises a plurality of memory locations.

27. (previously amended) The apparatus of claim 25 wherein each block of memory locations comprises a single memory location.

28. (currently amended) A system comprising

a controller to accept a plurality of descriptors, wherein the descriptors are received in a first order and wherein each descriptor includes a command and a memory address identifying a memory location external to the descriptor to which a completion status of the command will be written upon completion of the command;

a plurality of ~~computational~~ encryption units, wherein the units execute commands from the respective descriptors; and

a memory providing the memory locations,

wherein upon completion of a command included in a respective descriptor, the controller writes a respective completion status value for the command to the memory address external to the respective descriptor;

wherein the plurality of encryption units comprise (1) an Advanced Encryption Standard (AES) encryption engine; and (2) a Data Encryption Standard (DES) engine; and

wherein the controller comprises logic to write a second completion status to a memory address external to a second descriptor prior to writing a first completion status to a memory address external to a first descriptor and wherein controller logic to execute a command in the first descriptor is initiated before execution of a command in the second descriptor is initiated.

29. (cancelled) .

30. (original) The system of claim 28 wherein the commands are grouped into categories, and the completion status of commands in each category are written to different blocks of memory locations.

31. (original) The system of claim 30 wherein each block of memory locations comprises a plurality of memory locations.

32. (original) The system of claim 30 wherein each block of memory locations comprises a single memory location.

33. (currently amended) A computer implemented method comprising:

~~issuing~~ receiving a plurality of descriptors ~~to~~ at a controller, each operation descriptor comprising a command; and

initiating executing the commands in a first order; and

indicating a completion status of each command, as each command completes, in the order that it completes, which is different from the first order;

wherein at least some of the descriptors comprise commands executed by one of multiple encryption units implementing different respective encryption algorithms;

wherein the controller comprises the multiple encryption units; and

wherein the multiple encryption units comprise (1) an Advanced Encryption Standard (AES) encryption engine; and (2) a Data Encryption Standard (DES) engine; and

the controller comprises logic to write a second completion status to a memory address external to a second descriptor prior to writing a first completion status to a memory address external to a first descriptor and wherein controller logic to execute a command in the first descriptor is initiated before execution of a command in the second descriptor is initiated.

34. (previously presented) The computer implemented method of claim 33 wherein each descriptor further comprises a memory address identifying a memory location to which the completion status for its respective command will be written, and a value representing the completion status to be written upon completion of its respective command.

35. (cancelled).

36. (previously presented) The computer implemented method of claim 1 wherein each descriptor comprises a value to be written to the memory address identifying a memory location external to the descriptor upon completion of the command of the descriptor.

37. (cancelled).

38. (cancelled).

39. (previously presented) The article of manufacture of claim 12 wherein each descriptor comprises a value to be written to the memory address identifying a memory location external to the descriptor upon completion of a command of the descriptor.

40. (cancelled)

41. (cancelled) .

42. (cancelled).

43. (cancelled).

44. (currently amended) The ~~apparatus~~ network controller of claim 25 wherein each descriptor comprises a value to be written to the memory address identifying a memory location external to the descriptor upon completion of the command.

45. (cancelled).

46. (cancelled)

47. (previously presented) The apparatus of claim 30 wherein each descriptor comprises a value to be written to the memory address identifying a memory location external to the descriptor upon completion of the command of the descriptor.

48. (cancelled)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LeChi Truong whose telephone number is (571) 272-3767. The examiner can normally be reached on 8 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR of Public PAIP. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIP system, contact the Electronic Business Center (EBC) at 866-217-9197(toll-free).

LeChi Truong

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